

SMD ULTRA LOW CAPACITANCE UNI-DIRECTIONAL TVS FOR ESD PROTECTION DIODE, 5V

Top View Dimensions:
 Total width: 0.051 (1.30) / 0.043 (1.10)
 Lead width: 0.035 (0.90) / 0.028 (0.70)
 Lead height: 0.014 (0.35) / 0.009 (0.25)

Side View Dimensions:
 Lead height: 0.028 (0.70) / 0.020 (0.50)

Bottom View Dimensions:
 Total width: 0.067 (1.70) / 0.059 (1.50)
 Lead height: 0.007 (0.20) / 0.002 (0.05)

PRODUCT FEATURES

1. FLAMMABILITY CLASSIFICATION 94V-0
2. RESPONSE TIME <1ns TYP.
3. ULTRA LOW CAPACITANCE, 0.5pF TYP.
4. IEC COMPATIBILITY:
 IEC61000-4-2 (ESD) ±15KV (AIR), ±10KV (CONTACT)
 IEC61000-4-4 (EFT) 80A (5/50nS)
 IEC61000-4-5 (LIGHTNING) >1A (8/20µS)
5. LOW LEAKAGE CURRENT
6. CASE: TRANSFER MOLDED, SOD-523FL
7. DIMENSIONS IN INCHES AND (MILLIMETERS)
8. LEADS: SOLDERABILITY PER MIL-STD-750 METHOD 2026
9. WEIGHT: 0.002 GRAMS
10. RoHS COMPLIANT, ADD SUFFIX "H" FOR HALOGEN FREE
 i.e. ESD5L5.0-H: RoHS COMPLIANT/HALOGEN FREE

ELECTRICAL CHARACTERISTICS

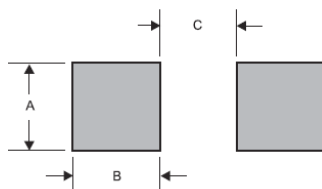
MAXIMUM RATINGS (T_A =25°C UNLESS OTHERWISE NOTED) AND ELECTRICAL CHARACTERISTICS

RATING	SYMBOL		UNITS
TOTAL POWER DISSIPATION, NOTE 1	P _D	0.2	W
TYPICAL THERMAL RESISTANCE	R _{θJA}	635	°C/W
	R _{θJC}	350	°C/W
STORAGE TEMPERATURE RANGE	T _{STG}	- 55 TO +150	°C
OPERATING JUNCTION TEMPERATURE RANGE	T _J	- 55 TO +125	°C

PART NUMBER	Max. V _{RWM} (V)	Max I _R @ V _{RWM} (µA)	Min V _{BR} @ I _T =1mA (A)	Max V _C @ I _{PP} =1A (V)	Max I _{PP} (A)	MAX P _{PK} (W) (NOTE 2)	MAX C _J (pF)	MARKING
ESD5L5.0	5.0	1	5.4	9.8	1	40	0.9	5L

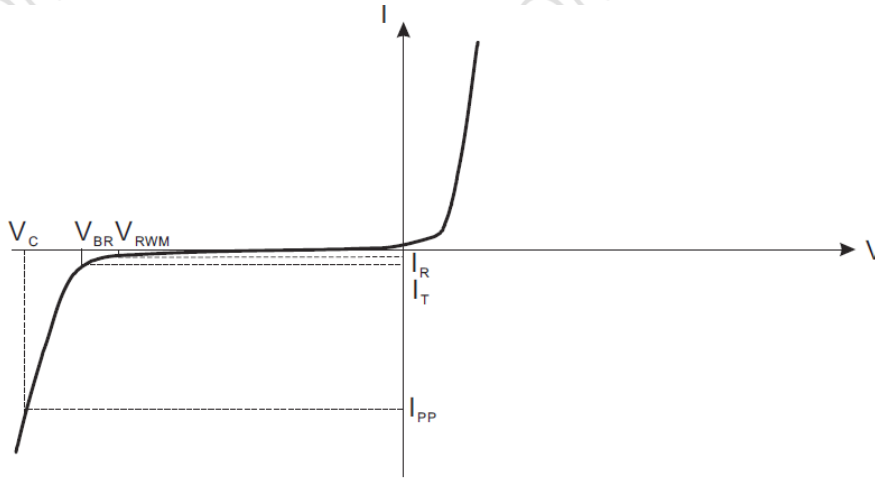
- NOTE : 1. ON 1"x0.75"x0.62" FR-5 PCB
 2. SURGE CURRENT WAVEFORM PER FIG 5.
 3. UNLESS SPECIFIED OTHERWISE, THE ELECTRICAL TEST IS PERFORMED AT T_A=25°C, V_F=1V@I_F=10Ma
 4. SEE FIGURE 3 AND 4 FOR TEST SETUP

LAYOUT RECOMMENDATION



PACKAGE	A	B	C
SOD-523FL	0.032 (0.80)	0.024 (0.60)	0.044 (1.10)

RATINGS AND CHARACTERISTIC CURVES



Uni-Directional TVS

- V_C : Clamping Voltage @ I_{PP}
- I_{PP} : Maximum Reverse Peak Pulse Current
- V_{RWM} : Maximum Working Peak Reverse voltage
- I_R : Maximum Reverse Leakage Current @ V_{RWM}
- V_{BR} : Breakdown voltage @ I_T
- I_T : Test Current
- P_{PP} : Peak Pulse Power
- C_J : Max. Capacitance @ $V_R = 0V$ and $f = 1MHz$

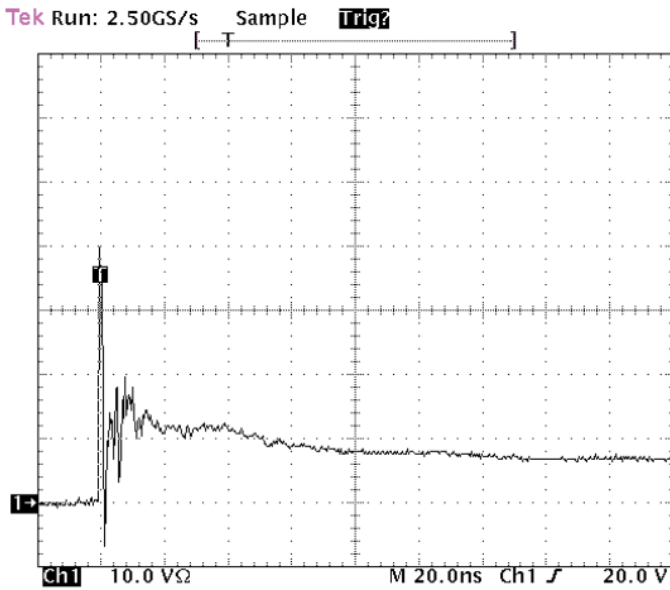


Figure 1. ESD clamping voltage screenshot
Positive 8 kV contact per IEC 61000-4-2

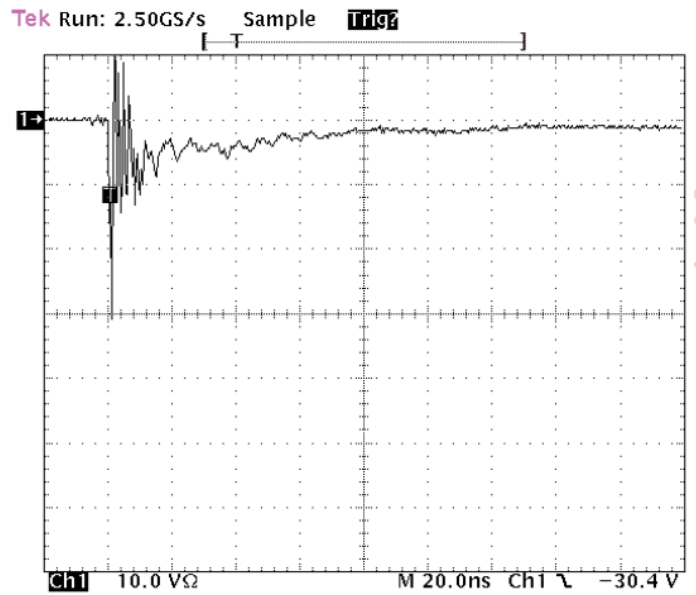


Figure 2. ESD clamping voltage screenshot
Negative 8 kV contact per IEC 61000-4-2

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

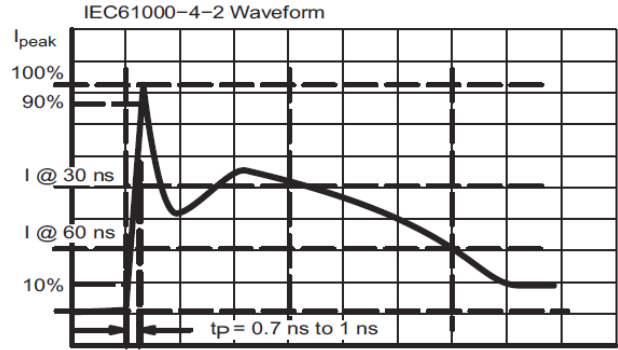


Figure 3. IEC61000 -4-2 Spec

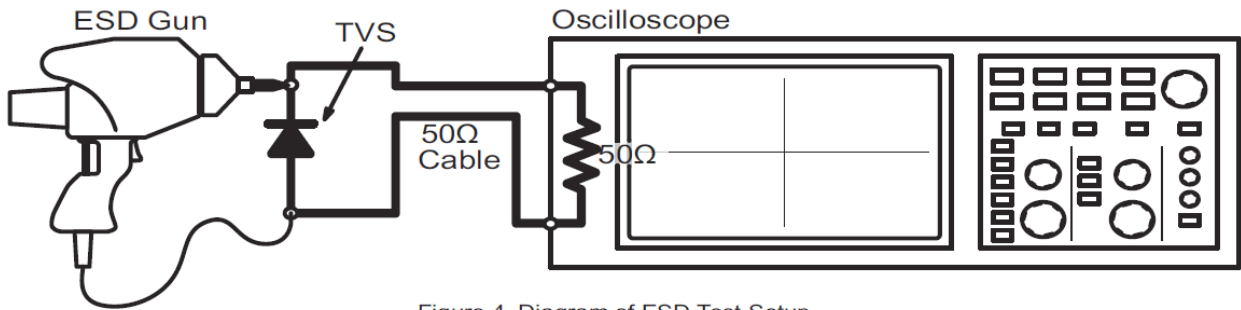


Figure 4. Diagram of ESD Test Setup

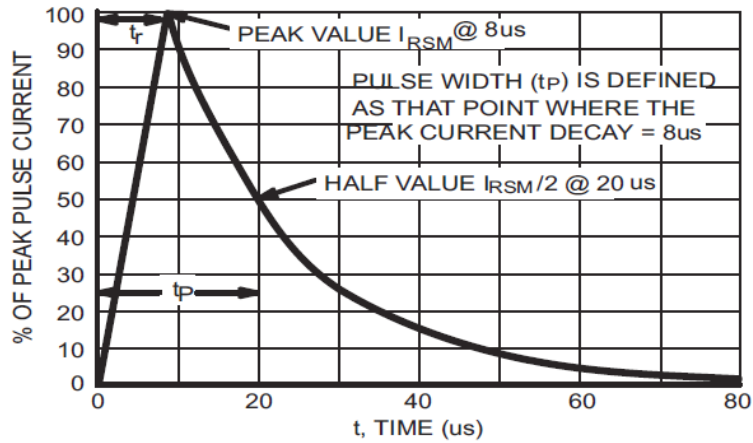


Figure 5. 8 X 20us Pulse Waveform